CBCS SCHEME

USN | | | | | | | | | | |

18ELD21

Second Semester M.Tech. Degree Examination, June/July 2019
Advanced Computer Architecture

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain Michael Flynn's classification. **(08 Marks)**
b. Explain Explicit parallelism and Implicit parallelism and Implicit parallelism. **(06 Marks)**
c. Explain Architecture of Vector super computer. **(06 Marks)**

OR

2 a. Explain Data and Resource dependences. **(08 Marks)**
b. Differentiate control flow versus Data flow architecture. **(06 Marks)**
c. Explain Bernstein's conditions. **(06 Marks)**

Module-2

3 a. Explain Mean performance of a multi mode computers. **(08 Marks)**
b. Explain Efficiency, utilization and Quality. **(06 Marks)**
c. Explain Scalability metrics. **(06 Marks)**

OR

4 a. Explain Virtual Memory models. **(06 Marks)**
b. Give IBM/6000 Superscalar processor architecture. **(08 Marks)**
c. Explain Inclusion , Coherence and Locality. **(06 Marks)**

Module-3

5 a. Explain Direct Mapping cache organization. **(08 Marks)**
b. Explain Sequential consistency model. **(06 Marks)**
c. Explain Interleaved memory organisation. **(06 Marks)**

OR

6 a. Explain Speed up, Efficiency and Throughput with respect to pipeline design. **(10 Marks)**
b. Explain Mechanism of Instruction pipelining. **(10 Marks)**

Module-4

7 a. Explain Vector processing principles. **(10 Marks)**
b. Explain CM – 2 Architecture. **(10 Marks)**

OR

8 a. Explain Latency hiding technique. **(10 Marks)**
b. Explain the principle of Multithreading. **(10 Marks)**

Module-5

9 a. Explain shared variable model. **(10 Marks)**
b. Explain Parallel Language Features for Parallelism. **(10 Marks)**

OR

10 a. Explain principles of Synchronization. **(10 Marks)**
b. Discuss shared variable program structures. **(10 Marks)**

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